

# Mohammadreza Alimadadi

Computer Science Department

Stony Brook University New York, US

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## Education

### Stony Brook University

*Ph.D. Candidate in Computer Science;*

– GPA: 3.76/4

– Research: Acceleration of Distributed System algorithms

– Graduate Courses: Computer Architecture - Operating Systems - Compilers - Data Science

New York, US

2018 – Present

### University of Tehran

*M.Sc. of Computer Engineering, Computer Architecture;*

– GPA: 17.01/20 (3.67/4.0)

– Thesis: High Level Synthesis of Approximate Computing Circuits

Tehran, Iran

2014 – 2017

### Iran University of Science and Technology

*B.Sc. of Electrical Engineering, Electronics;*

– GPA: 16.07/20 (3.29/4.0)

– Thesis: Image Encryption using Wavelet Transform

Tehran, Iran

2009 – 2014

## Research Interests

- **Hardware Acceleration**
- **Computer Architecture**

## Research Experiences

### Research Assistant at *COMPAS Lab*

*Stony Brook University, US*

2018 – Present

### Research Assistant at *High Performance Embedded Architecture Lab*

*University of Tehran, Iran*

2014 – 2018

### Undergraduate Research Assistant at *Dependable Systems Lab*

*Iran University of Science and Technology, Iran*

2012 – 2014

## Work Experiences

### **Researcher & Designer, HooshRavan**

*Embedded System Developer & PCB Designer*

2016 – 2017

### **Researcher & Designer, Hamayeh Corporation**

*Embedded System Developer & PCB Designer*

2012 – 2015

### **Chairman, Robotic Scientific Association**

*Iran University of Science and Technology*

2011 – 2012

## Selected Projects

### **Waverunner: A Hardware Accelerator for Raft Consensus Algorithm**

*We designed a microsecond latency and high throughput hardware accelerator for Raft*

2020 – Present

### **Hardware Accelerator for Distributed Hash based on Chord Algorithm**

*We are designing an hardware accelerator based on Chord to achieve low latency.*

2021 – Present

**Version Control File System***Implement version control file system like git in the kernel*

Operating Systems

2019

**5-Stage Pipeline RISC-V***Implement 5 stage pipeline RISC-V with System Verilog*

Computer Architecture

2019

**Chaos-based Image Encryption Accelerator***Implement the accelerator for Nios II processor on Altera FPGA*

Embedded Systems

2015

**Workload Characterization***Profile MiBench and PARSEC benchmarks On GEM5 and study the effect of acceleration*

2017

**Tag-less Cache for First-Level Cache Power Reduction***Implement with VHDL*

Computer Architecture

2014

**Technical Skills****Programming:**

Expert in C/C++

Expert in Verilog &amp; VHDL

Good at Python

Worked with Boost Library

Worked with DPDK Library

**Tools & CAD:**

Expert in Vivado &amp; Quartus

Expert in Vivado HLS

Good at Design Compiler &amp; Power Compiler

Worked with Intel VTune &amp; Valgrind

Worked with LLVM

Worked with GEM5 &amp; MARSS

**References****Michael Ferdman***mferdman@cs.stonybrook.edu***Shuai Mu***shuai@cs.stonybrook.edu*