Shenghsun Cho

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EDUCATION

Ph.D. Candidate, Computer Science, Stony Brook University, NY, U.S.A. Aug.2013 – Spring.2021 (expected)
- Research in computer architecture, operating systems, FPGA, and accelerators. Advisor: Prof. Mike Ferdman

M.S., Electrical Engineering, National Taiwan University, Taiwan Sep.2005 – Jun.2007
- Research in embedded systems, digital design, and network packet processing. Advisor: Prof. Sheng-De Wang

B.S., Computer Science, National Central University, Taiwan Sep.2000 – Jun.2005

SKILLS

- System software programming: C, Python, Linux kernel, Linux device driver, RISC-V
- Computer system architecture: PCIe, memory, network, design/analysis/debug across software and hardware
- FPGA digital design: Verilog, SystemVerilog, SystemC, Vivado HLS, VCS, Verdi, Quartus, Vivado, Synplify

INDUSTRY EXPERIENCE

Intern, software for next-generation interconnect, AMD Research, MA, U.S.A. Mar.2018 – Aug.2018
- Device driver and MPI program development for next-generation interconnect that aims to replace PCIe.

Intern, FPGA for data centers (Catapult project), Microsoft Research, WA, U.S.A. Jun.2015 – Aug.2015
- Multi-FPGA communication using OpenCL.

Senior engineer, software/hardware for digital IPs, Global Unichip Corp., Hsinchu, Taiwan Oct.2007 – Jun.2013
- Embedded software: Standalone program and Linux device driver for ARM SoC.
- Software/hardware co-design: Transactor that links virtual software platform and physical FPGA circuit as a single ARM SoC emulator.
- High speed interface digital IP: 720MHz LVDS digital IP design with wire skew control within picosecond level.
- ASIC tape-out: LVDS 65nm/40nm customer ASIC. V-By-One HS test chip.

PROJECTS (selected)

Host-Accelerator Communication in Heterogeneous-ISA environments Jun.2014 – Present
- Design a fast and easy-to-use software programming interface between host and accelerators.
- Enable generic virtual memory support for PCIe based accelerators.
- Reduce software thread migration overhead of heterogeneous-ISA multi-core systems to 23x less than prior work.

Microsecond-Level Device Access Mar.2017 – Oct.2018
- Study and analyze the bottleneck for current software/hardware when accessing emerging microsecond-level devices.
- Enhance a user-space threading library with software prefetch and request/response queues to hide microsecond-level latencies.
- Design and implement a PCIe connected storage emulator with controllable access latency using FPGA.

Accelerator Designs on FPGAs Dec.2013 – Present
- Design an explicit state model checker using FPGA. Achieve near 1000x speedup over software.
- Research on offloading entire Linux TCP/IP stack to FPGA to save power while retaining full functionality.

PUBLICATIONS (selected, first author only)

Flick: Fast and Lightweight ISA-Crossing Call for Heterogeneous-ISA Environments (ISCA 2020)
Shenghsun Cho, Han Chen, Sergey Madaminov, Michael Ferdman, Peter Milder*, in 47th International Symposium on Computer Architecture (ISCA), 2020.*

Taming the Killer Microsecond (MICRO 2018)
Shenghsun Cho, Amoghavarsha Suresh, Tapti Palit, Michael Ferdman, Nima Honarmand, *in 51st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2018.*

FPGASwarm: High Throughput Model Checking on FPGAs (FPL 2018)
Shenghsun Cho, Michael Ferdman, Peter Milder, *in 28th International Conference on Field Programmable Logic and Applications (FPL), 2018.*

A Full-System VM-HDL Co-Simulation Framework for Servers with PCIe-Connected FPGAs (FPGA 2018)
Shenghsun Cho, Mrunal Patel, Han Chen, Michael Ferdman, Peter Milder, *in Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), 2018.*

PATENTS

Dynamic virtualized field-programmable gate array resource control for performance and reliability
David A. Roberts, Shenghsun Cho, US Patent 10,447,273.

Method and system for packet classification with reduced memory space and enhanced access speed
Shenghsun Cho, Sheng-De Wang, US Patent 7,953,082.