Zavosh Mottahedeh

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Interests

- ◇ Computer Architecture
- ◇ FPGA
- ◇ GPU and Accelerators
- ◇ Neural Networks

Education

◇ Ph.D. in Computer Science — 2019 – present
Stony Brook University, NY, US — **GPA: 3.92/4.00**

Courses: Analysis of Algorithm (A), Operating Systems (A), Computer Architecture (A), Hardware Architectures for Deep Learning (B+), Distributed Systems (A-), Natural Language Processing (A-).

◇ B.Sc. in Computer Engineering, Computer Architecture — 2015 – 2019
Sharif University of Technology, Tehran, Iran — **GPA: 18.88/20.00**

Relevant Courses: Logical Circuits Design (19.6/20), Digital Systems Design (19.2/20), Computer Structure & Language (18.6/20), Computer Architecture (20/20), Microprocessor (19.5/20), VLSI Design (19.3/20), Multi-core Computing (18.7/20).

Research and Working Experiences

◇ **Research Assistant**, Stony Brook University, NY, US — 2019 – present

– **Argus** is an end-to-end framework for accelerating Convolutional Neural Networks (**CNN**s) on **FPGA**s. The core of Argus is an accelerator generator that translates high-level CNN descriptions into efficient multi-core accelerator designs. Argus explores an extensive design space, jointly optimizing all design aspects for the target FPGA and generating multi-core accelerator designs that achieve near-perfect dynamic arithmetic unit utilization.
I made Argus compatible with High-Bandwidth Memory (**HBM**) to resolve Argus' off-chip memory bandwidth bottleneck by storing CNN weights on HBM. I have implemented support of Fully-connected layers, Global Average Pooling layers, and Depth-wise Convolution layers for Argus. I also fused Depth-wise Convolution to regular convolution in order to reduce off-chip feature-map data transfer. Currently, I am implementing a line-buffer fusion method which can fuse multiple CNN layers.

◇ **Intern**, Noavaran Amn Andish Sharif Corporation (NAADSec), Tehran, Iran — 2018

– Implemented a **python API** using **SWIG** tool for an FPGA-based hardware security module.

Honours and Awards

◇ **First place** in **Sharif FPGA Challenge** — 2017

– Implemented a **Trax Game player** on an **Altera DE2** board using **Verilog HDL**, based on the paper "Highly efficient alpha-beta pruning minimax based Loop Trax Solver on FPGA"

◇ **Silver** Medal of **National Olympiad** on Astronomy and Astrophysics. — 2014

◇ **Bronze** Medal of **National Olympiad** on Astronomy and Astrophysics. — 2013

Skills

- ◇ **Programming & Data-Base Langs**: Python, C/C++, Java, Go, R, Matlab, Postgre SQL
- ◇ **HPC APIs**: CUDA, OpenMP
- ◇ **HDL & Assembly**: HLS, Bluespec, System Verilog, Verilog HDL, MIPS and 8086 assembly
- ◇ **Micro-controllers**: Raspberry pi, Arduino
- ◇ **Hardware Tools**: Modelsim, Xilinx Vitis/Vivado/ISE/SDK, Quartus, Proteus, Simple Scalar
- ◇ **Network & Other Tools**: GNS3, Wireshark, Packet Tracer, Git, CMake, SWIG

Notable Course Projects

- ◇ Implemented a **RAFT**-based **Distributed** Key-Value system using **Go**.
- ◇ Implemented a **RISC-V** core with ability of running **Linux** using **System Verilog**.
- ◇ Implemented a **Clustering** algorithm on an **NVIDIA GPU** using **CUDA**.
- ◇ Redesigned and implemented the **basic multi-cycle processor** in M. Morris Mano's "Computer System Architecture" using **Verilog HDL**.
- ◇ Implemented a code that applies a **filter** on **BMP** pictures on an **NVIDIA GPU** using **CUDA**, and calculated and analyzed its **speed-up** in various sizes of input pictures in comparison with running the same algorithm on CPU.
- ◇ Designed and implemented a **RISC ISA** in the **single-cycle**, **multi-cycle** and **pipeline** (including **Hazard Detection** and **Data Forwarding**) architectures using **Quartus Schematic**.
- ◇ Studied different **cache sizes**, **block sizes**, **associativities**, and **replacement policies** of **instruction cache** and **data cache** using **Simple Scalar** to compare and analyze trends of **miss rate** and **AMAT**.
- ◇ Designed and implemented an **AES** module using **Verilog HDL**.

Teaching Assistantships

◇ Stony Brook University, NY, US

- **System Fundamentals I**, Prof. McDonnell 2023
- **System Fundamentals II**, Prof. Stark 2020

◇ Sharif University of Technology, Tehran, Iran

- **Compiler Design**, Prof. Ghassem-Sani 2018
- **Computer Structure and Language**, Prof. Asadi 2018
- **Digital Systems Design**, Prof. Bayat-Sarmadi 2017
- **Logical Circuits Design**, Prof. Bayat-Sarmadi 2017

Volunteer Experiences

◇ Stony Brook University, NY, US

- Gained **long-term leadership** and **teamwork** experience by being president of Iranian Graduate Student Association since 2022.

◇ Sharif University of Technology, Tehran, Iran

- Gained **short-term team management experience** through **leading** FPGA section of two university-wide hardware-focused competition events, Gatuino Challenge 2018 and HardWar 2019.
- Gained **short-term team-work experience** through staffing in two talk-based events, SLANT 2018 and TEDxSUT 2019.